

## 3.5 GHz Bandwidth Low-Cost GaAs IC Receiver for 2.5 to 5 Gbit/s Optical Links

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**Abstract:** This paper describes the main issues of a work which permitted development, optimization and fabrication of wideband packaged optical receivers for 2.5 to 5 Gbit/s optical links, having extremely low costs. A description of the manufacturing technologies we employed in the final product fabrication, various typical receiver performances as well as its cost analysis are also reported.

### I. INTRODUCTION

High bit rate optical links play, as well known, a role of fundamental relevance in telecommunication development. Moreover, owing to a big and increasing customer demand for high speed digital services, optical equipment and product suppliers are now extremely interested in using very wide band networks [1,2]. The major difficulty for achieving this goal has been, until now, constituted by the relatively high costs involved [1]. In this paper we describe and discuss the main issues of the development procedure we used for producing high sensitivity packaged optical receivers for application in 2.5 to 5 Gbit/s links with an extremely low cost.

This goal was achieved through this sequence of steps: 1- development, on the basis of a new design method of a small size ( $1.3 \text{ mm}^2$ ) GaAs MMIC transimpedance amplifier, optimized for mass production, having high yields and performances (bandwidth, noise and dynamic range). 2- development of a very cheap hybrid receiver assembly by using a proprietary and advanced low cost multichip module (MCM) technology. 3- receiver assembly mounting on a standard butterfly package (Tekform Inc.).

So, the paper will first report the main design, performances and producibility issues of the developed transimpedance amplifier (TIA) MMIC. Then, it will describe the basic features of the proprietary MCM technology used in the packaged receiver fabrication. A receiver cost analysis will be finally reported.

### 2. DESIGN, PERFORMANCE AND PRODUCIBILITY ISSUES OF THE DEVELOPED WIDEBAND MONOLITHIC TRANSIMPEDANCE AMPLIFIER.

State of the art low frequency TIA circuits are usually constituted by a cascade of relatively complex stages [3], while very wide band circuits make use of a simpler topology where the amplifying action is performed by one single transistor (here called single device inverter, SDIs). Because of the need of low feedback resistors, SDIs have a poor noise performance. A consistent noise improvement and various other advantages [4] were obtained, while maintaining a wide band performance, substituting the SDI by a cascode inverter. Cascode type TIA MMICs were extensively reported in the literature [5,6,7,8,9,10].

If examined for a large volume production, almost all the cascode type MMICs available in the literature show yield and size limitations. In fact, these circuits have a relatively low d.c. yield because of the high number of their elements (corresponding to a big total on chip gate width) and a poor r.f. yield because the d.c. voltage on the output of the cascode stage is very sensitive to the process fluctuations. If the cascode drives other amplifying stages, as in the above references from [5] to [10], these voltage variations often determine an incorrect r.f. working of the following stages, by damaging amplifier gain, bandwidth or dynamic range. We proved this point through a systematic yield study performed by using TriQuint foundry data sets on process fluctuation and the ref. 11 method for yield calculation with the relevant models. This situation outlined the opportunity of setting up and publishing a new full design method especially tailored on the development of low-cost mass producible monolithic TIAs. By starting from the achievements of ref. 11, we developed such a method, which permitted the



design of the TIA MMIC constituting the core of our low-cost packaged receivers. Their intrinsic performance advantages were described in references 12 and 13, while the newly developed design method and the circuit issues allowing a very high overall yield were reported in ref. 14. The circuit solution, permitting a careful gain and peaking amplitude control as a function of the process fluctuation was also patented [15] and various patent international extensions are pending. For reaching very high d.c. and parametric yields, we developed a  $1.15 \times 1.15 \times 0.2 \text{ mm}^3$  chip having 8 transistors and 1 diode only, where the cascode is directly connected to the amplifier output buffer which can easily follow the voltage variations without r.f. performance degradation. The total on chip gate width was reduced to less than 1.4 mm and only 3 vias were used. Circuit topology is shown in fig. 1.

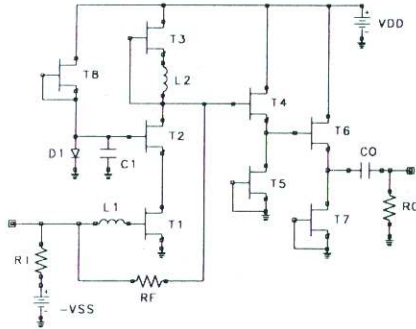


Fig. 1: Schematic diagram of the TB40D32 IC.

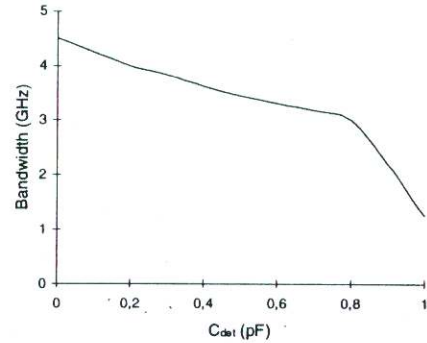


Fig. 2: TIA bandwidth x photodiode capacitance.

A double inductor peaking is used, which allows an expressive widening of the transimpedance bandwidth to be obtained. Inductance  $L_1$  produces an increase with the frequency of the amplifier voltage gain by resonating the input capacitance of the transistor  $T_1$ , so compensating for the feedback current reduction due to the input shunting action of the detector diode parasitic capacitance. Inductance  $L_2$  increases the high frequency load of the cascode stage and reduces the noise fluctuations of the current passing into the amplifying devices. The extraordinary broadening of the achievable bandwidths, due to the simultaneous peaking action of the inductor couple, permits the use of very high feedback resistors, so allowing a strong reduction of the amplifier equivalent input noise current density. For this reason our circuit, which, by using the same technology (GEC-Marconi 0.5  $\mu\text{m}$  GaAs MESFETs, F20 process), has a transimpedance bandwidth twice than those of the above mentioned designs, still shows a better equivalent input noise current density. This explains why when using the circuit (designed and optimized for 5 Gbit/s operation) in 2.5 Gbit/s optical receivers an improvement of about 2 dB in the measured sensitivity is obtained with respect to the ref. 8 results. Noise reduction and greater simplicity of our topology also permit a reduction of the ratio between the amplitude of the minimum detectable signal and the maximum linear signal amplitude, so resulting in a dynamic range improvement, as explained in [16]. Our MMIC guarantees a correct receiver operation at 2.5 Gbit/s even with high capacitance low-cost photodiodes, as can be observed in fig. 2 where the receiver bandwidth dependence on the photodiode parasitic capacitance is given. Table 1 shows a comparison between measured performances of our TIA circuit (TB40D32), when loaded at the input with a 0.5 pF capacitance, and those of the Anadigics GaAs MESFET product showing the widest analogical bandwidth (ATA 30011), when loaded with a 0.4 pF input capacitance. Fig. 3 shows the measured bandwidth of the receiver.

Table 1: Comparison with two TIA ICs.

Characteristics	ATA30011 (C <sub>det</sub> 0.4pF)	TB40D32 (C <sub>det</sub> 0.5pF)
Transimpedance gain (dBΩ)	58.5	59
Transimpedance bandwidth (GHz)	2.5	3.5
Input noise density at 1.4 GHz (pA/Hz <sup>1/2</sup> )	10.8	6
Electrical dynamic range (dB)	40	51

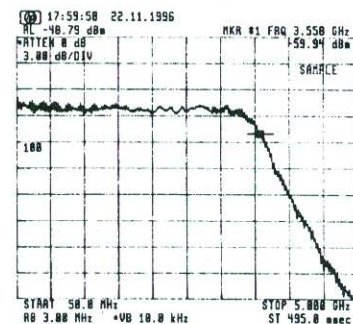


Fig. 3: Output voltage bandwidth with -12dBm input optical power.

The observed cutoff frequency, higher than 3.5 GHz, fully enables the receiver for use in 5Gbit/s links. Fig. 4 shows the receiver BER measured at 2.5 Gbit/s and fig. 5 gives the relevant eye diagram.

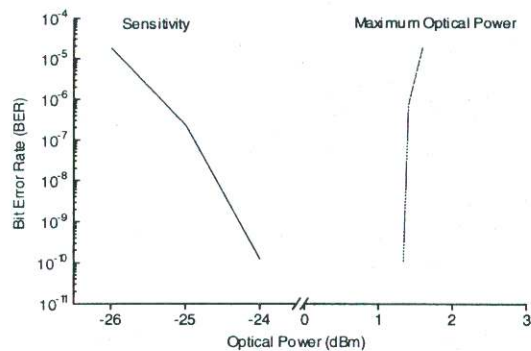


Fig. 4: BER measurement for minimum and maximum input optical power at 2.5 Gbit/s.

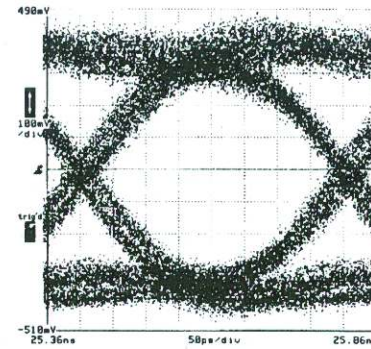


Fig. 5: Eye diagram for -12dBm input optical power including low-pass filter.

Fig. 6 gives the measured receiver equivalent input noise current density while fig. 7 shows a sketch of the packaged receiver and its pinout. A butterfly type package from Tekform Inc. was used.

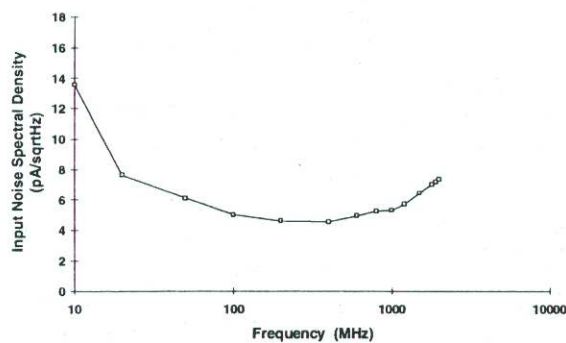


Fig. 6: Measured equivalent input noise current spectral density.

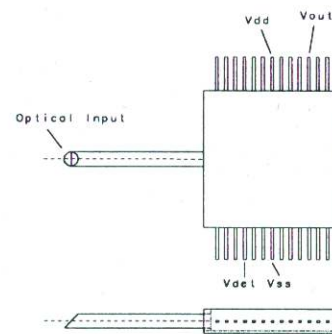


Fig. 7: Optical receiver package - Butterfly.

### 3. MCM TECHNOLOGY AND COST ANALYSIS

The packaged receiver makes use of a hybrid alumina substrate manufactured with a proprietary low-cost (less than US\$1.50 per square inch) MCM technology, which was described in detail in [17]. Copper or copper/gold conductor layers are plated using a specific nickel deposit as adhesion layer onto the ceramic substrate. Their patterning is made using dry-film and wet etching. The above cost was determined for our in house pilot line and material, laboratory equipments, labour and Telebrás over head were included. Important factors in determining this result were the type of process for film deposition. Although our technology does not present integrated resistors yet, it must be observed that the cost per chip resistor is very low (units of cents) and in microwave circuits only few resistors are used (loads, bias filters, attenuators,...), consequently this contribution in the final cost is not significant. Table 2 shows a cost comparison between our technology and other types of technologies available in the market [17].

Table 2: Hybrid technology comparison.

Technology	Cost/in <sup>2</sup> (US\$)	Comments
Thin Film	12.00 - 14.00	with metallized vias, integrated resistors
Thick Film	2.50 - 3.80	no metallized vias, integrated resistors
Soft Substrate	2.30 - 2.80	with metallized vias
TELEBRÁS MCM Technology	< 1.50	with metallized vias



Considering the prototypes manufactured single piece cost was predicted around US\$1,000.00. This is a very attractive value if compared with other solutions available at the market and certainly in production volume this value shall be lower.

#### 4. CONCLUSIONS

The main issues of a work which permitted the full development of very low-cost GaAs packaged optical receivers for 2.5 to 5 Gbit/s optical links have been described. Particular relevance has been given to put into evidence the design concepts permitting a substantial saving in the final product fabrication. Finally, a cost evaluation has been given.

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